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COMMON SYSTEMS

PROGRAMMABLE
READ ONLY MEMORY
CIRCUIT

SECTION I - GENERAL DESCRIPTION

1. PURPOSE OF CIRCUIT

1.01 The programmable read only memory (PROM) circuit is used in the 3A central control (CC). The 3A CC is a microprogrammed processor utilizing PROMs for its microprogram store. This microstore contains up to 4096 32-bit words. Each microstore circuit pack (CP) contains four PROMs; each PROM is 1024 words by 4 bits. These memories are arranged for a CP organization of 1024 words by 16 bits. Two of these CPs are read out in parallel to obtain a 32-bit microprogram word. The basic building block of the microstore, then, is 1024 32-bit words, which are contained on two CPs.

SECTION II - DETAILED DESCRIPTION

1. ADDRESS BUFFER

1.01 The selection of a word in the microstore is performed in two steps. First, address bits 0 through 8 of the processor's microprogram store address register (MAR) are bused to all of the microstore CPs. The decoding of these nine address bits is performed on each CP for a one of 512-word selection. Concurrently, address bits 9 through 11 of the MAR are decoded in the processor and a plane select is generated. This plane select lead is designed for the enabling of a pair of microstore CPs containing the 32-bit microprogram word.

1.02 Address information to the microstore CP is derived from the processor's 3-volt collector diffusion integration (CDI) logic. Since all of the devices in the microstore are 5-volt TTL (transistor-transistor logic), an interface is required. This interface is performed on the address and plane select leads by using 3-volt pull-up resistors (R1 to R11) at the input of the buffers in the microstore. Each input to the microstore is driven by a MAR gate on a 1024-word basis. Each gate must drive two of the microstore CPs.

1.03 Address input bits to the microstore circuit, A0 through A8, are pulled up to 3 volts through 470-ohm resistors, then they are buffered and inverted in IC2 and IC3. Finally, these address bits are paralleled to address inputs A0 through A8, respectively, for all four PROMs. Each

PROM decodes these nine address bits for a one of 512-word selection.

1.04 Plane select inputs to the microstore circuit pack, designated as plane select low (PSL) and plane select high (PSH), are pulled up to 3 volts through 470-ohm resistors. These two signals are then logically combined in IC2 and IC3 to generate the A9 input and the two CS inputs of the PROMs. The logical combinations which exist are as follows: When PSL is enabled (low) and PSH is disabled (high), A9, which is high, selects the lower 512 words of the PROMs. When PSH is enabled and PSL is disabled, A9, which is low, selects the upper 512 words of the PROMs. When either PSL or PSH is enabled, both CS inputs of the PROMs are enabled (low), allowing data to be gated onto the microstore output bus. When PSL and PSH are disabled, both CS leads on the PROMs are disabled (high), preventing the transfer of the PROMs' data onto the microstore output bus. PSL and PSH should never be enabled simultaneously. This illegal state would cause data to be outputted onto the microstore output bus at the same time that another microstore CP is selected.

2. MEMORY

2.01 The memory used in the microstore is comprised of four PROMs. These devices are specified as KS-21951 L1, L2, or L3. Although three list numbers are shown for the PROMs, each PROM has only one list number. Only PROMs with the same list number are allowed on the same CP.

2.02 The PROMs are Schottky bipolar devices, each containing 4096 memory cells. Data content within the cell is determined during the programming of the devices. Programming is accomplished by passing an applied current through a selected fusible link. Each memory cell has an associated fusible link. The binary value of the cell is determined by the link being open or left intact. List 1 and List 3 devices use nichrome material for the fusible link. List 2 devices use a polycrystalline silicon material. The selection of four of the 4096 memory cells within the PROMs is performed in two steps. First, while six of the address bits are selecting one of 64 rows of cells, the remaining four address bits are selecting one of 16 columns of cells. In the second step, the chip-selects allow the contents of the four memory cells to be gated onto the outputs of the device.

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2.03 At the output of the microstore, a voltage interface is required since the PROM devices are 5-volt TTL and the logic in the processor is 3-volt CD1. This interface is accomplished by using PROM devices with open collector outputs which can be pulled up to 3-volt logic levels by processor logic.

SECTION III - REFERENCE DATA

1.01 None.

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DEPT 5515-LT-LEG

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COMMON SYSTEMS

TOLL POWER DISTRIBUTING UNIT
CIRCUITFOR USE WITH NO. 2 ESS,
2A ESS, 3 ESSSECTION I - GENERAL DESCRIPTION1. PURPOSE OF CIRCUIT

1.01 This circuit provides a focal point in the toll frame lineup for the distribution of -48 volt power from the ESS power plant.

2. GENERAL DESCRIPTION OF OPERATION

2.01 This circuit connects all toll circuits requiring -48 volt power to the appropriate power bus through distributing fuses.

SECTION II - DETAILED DESCRIPTION1. GENERAL

1.01 This circuit is located in a self-contained power distributing unit for mounting in an in-line toll frame. Power is distributed to the various equipment frames from the dual buses via the two -48 volt power distributing circuits. The maximum current capacity is 200 amperes for each bus.

2. DISTRIBUTING CIRCUIT - FS 1

2.01 FS 1 shows the distributing circuit. Fuses designated (-)0 are nonalarm-type fuses which connect the -48 volt buses to the using circuits via the power distributing circuit. The number and capacity of distributing fuses provided must be within the limits specified in Circuit Note 102. The available combinations within these limits are shown in detail in the equipment design requirements. Fuses designated (-)1 are alarm-type fuses rated at 1 1/3 amperes. Each power distributing fuse is shunted by a separate 1 1/3 ampere (alarm) fuse. When a distributing fuse blows, the associated alarm fuse also blows. The blown fuse (alarm) in turn applies -48 volts to the fuse alarm (FA) relay in the fuse alarm circuit (FS 3) through resistor FA0, FA1,

FA2, or FA3. The resistor protects the lead to the FA relay from excessive current which would otherwise occur if a trouble ground appeared on the lead at the same time a blown fuse applies power to the lead. It also limits the current through the relay windings.

3. FILTER CAPACITORS - FS 2

3.01 FS 2 shows the filter capacitors. Identical filters are used for the -48 volt buses. Each filter bank consists of three 12,000 UF capacitors wired in parallel. A 30-ampere nonalarm fuse in series with each capacitor protects the power bus from excessive current due to a shorted capacitor or trouble ground. Each nonalarm-type capacitor fuse is shunted by a separate 1 1/3 ampere alarm fuse. When a capacitor fuse blows, the associated alarm fuse also blows. The blown alarm fuse in turn applies -48 volts to the FA relay through resistors FA4 and FA5.

4. FUSE ALARM CIRCUIT - FS 3

4.01 FS 3 provides fuse alarm facilities for the distributing circuit (FS 1). A nonalarmed -48 volt fuse (PD) provides voltage to the PWR OFF lamp.

4.02 A voltage appearing on either -48 volt lead resulting from a fuse failure (FS 1) will operate the FA relay. Contacts on the relay:

- (a) Light the power-off lamp
- (b) Signal the scanner applique circuit
- (c) Signal the major alarm to the office alarm circuit (both audible and visual) through leads ABG and MJ and leads MJV and MJVR.

4.03 Removal of the blown alarm fuse will deactivate the alarm and reset the fuse alarm relay.

5. DISTRIBUTING CIRCUIT - FS 4

5.01 FS 4 is the distributing circuit for the 20-30 ampere fuses. The operation is similar to FS 1 with the alarm signal applied to the alarm relay through resistors FA6 and FA7. As before, the resistor limits the current through the relay coils.

SECTION III - REFERENCE DATA1. WORKING LIMITS

1.01 The maximum current per bus is 200 amperes.

2. FUNCTIONAL DESIGNATIONS2.01 Lamps

<u>Designation</u>	<u>Meaning</u>
PWR OFF	Power off, fuse blown

3. FUNCTIONS

3.01 Connects all toll frames requiring -48 volts to the appropriate power bus.

4. CONNECTING CIRCUITS

4.01 When this circuit is listed on a keysheet, the connecting information thereon should be followed.

- (a) Control Frame Circuit - SD-3H902-01 (Office Alarm Circuit).
- (b) -48 Volt Power Distributing Circuit - SD-3H907-01.

5. MANUFACTURING TESTING REQUIREMENTSIntermediate Requirements

5.01 None.

End requirements

5.02 This circuit should be tested to verify that it is wired in accordance with the schematic and wiring drawings, that the requirements of the circuit requirements table are met, and that the circuit is capable of performing all functions stated in this circuit description.

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